AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to ~~change a frequency of one or more~~ generate a plurality of first clock signals, each having a frequency determined in response to one or more first control signals;

a second circuit configured to generate said one or more first control signals and a second control signal in response to a data signal and a second clock signal; and

a third circuit configured to generate a first reset signal in response to either said second control signal or a predetermined time period expiring.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said one or more first control signals are configured to program said frequency of said ~~one or more~~ plurality of first clock signals.

3. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~one or more~~ plurality of first clock signals are generated ~~by~~ with one or more phase lock loop circuits.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 3, wherein said one or more first control signals are

configured to program at least one of said one or more phase lock loop circuits.

5. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~one or more~~ plurality of first clock signals are generated using a divider network.

6. (ORIGINAL) The apparatus according to claim 1, wherein said predetermined time period is programmable.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second circuit is further configured to generate a third control signal and said predetermined time period is started in response to said third control signal.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said third circuit further comprises a watchdog timer circuit configured to measure said predetermined time period in response to said third control signal.

9. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein one of said ~~one or more~~ plurality of first clock signals is presented to a clock input of a processor and said first reset signal is presented to a reset input of said processor.

10. (CURRENTLY AMENDED) The apparatus according to claim 9, wherein said ~~one or more first control signals~~ data signal and said second clock signal are generated using a number of instructions executed by said processor.

11. (ORIGINAL) The apparatus according to claim 10, wherein said instructions are contained in a computer readable medium.

12. (ORIGINAL) The apparatus according to claim 10, wherein said instructions are part of a basic input output system (BIOS) routine.

13. (ORIGINAL) The apparatus according to claim 9, wherein said predetermined time period expires only when said processor hangs.

14. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said third circuit is further configured to generate ~~a~~ a second reset signal in response to the expiration of said predetermined time period.

15. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second circuit comprises an inter-integrated circuit (I^2C) interface circuit.

16. (CURRENTLY AMENDED) ~~The~~ An apparatus ~~according to claim 1, wherein~~ comprising:

a first circuit configured to change a frequency of one or more clock signals in response to one or more first control signals, wherein said first circuit further comprises a logic circuit configured to control a skew of each of said one or more ~~first~~ clock signals in response to a ~~third~~ second control signal; ~~and~~

~~said~~ a second circuit ~~is~~ configured to generate said one or more first control signals, said second control signal and a third control signal; and

a third circuit configured to generate a first reset signal in response to either said third control signal or a predetermined time period expiring.

17. (ORIGINAL) The apparatus according to claim 16, wherein said skew is programmable.

18. (CURRENTLY AMENDED) An apparatus comprising:

means for ~~changing a frequency of one or more~~ generating a plurality of first clock signals, each having a frequency determined in response to one or more first control signals;

means for generating said one or more first control signals and second control signal in response to a data signal and second clock signal; and

means for generating a reset signal in response to either said second control signal or a predetermined time period expiring.

19. (CURRENTLY AMENDED) A method for recovering in a phase lock loop circuit from a processor hang due to over-clocking comprising the steps of:

(A) ~~changing a frequency of~~ generating a plurality of first clock ~~signal~~ signals, each having a frequency determined in response to one or more first control signals;

(B) generating said one or more first control signals and a second control signal in response to a data signal and a second clock signal, wherein said processor is reset in response to said second control signal when said frequency is changed; and

(C) detecting whether said processor hangs in response to said frequency change.

20. (CURRENTLY AMENDED) The method according to claim 19, further comprising the step of:

(D) when said processor hangs, changing said frequency of said plurality of first clock ~~signal~~ signals to a fail-safe frequency and resetting said processor.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 14, wherein:

said first reset signal is configured to reset a processor; and

said second reset signal is configured to reset an entire system.